Journal of Engineering and Applied Research (JEAR)

National University of Skills

Summer & Autumn 2024, Vol. 1, No. 2, p. 179-197

Journal Homepage: https://jear.tvu.ac.ir/

doi:10.48301/JEAR.2024.459244.1029

16-channel Wireless Implantable Neural Recording Microsystems Based on Frequency-division Multiplexing

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ARTICLE INFO

Article Type:
Original Research

Received: 06.26.2024
Revised: 09.16.2024
Accepted: 09.24.2024

Keyword:
Microsystem
Neural Recording
Implantable
Frequency Division Multiplexing

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ABSTRACT

In the present paper, a 16-channel implantable wireless neural recording system is presented. The proposed system employs frequency-division multiplexing (FDM) to transfer multiple neural channels to an external setup wirelessly. The main advantage of the proposed system is that, while increasing the number of channels, it efficiently utilizes the limited bandwidth allocated for wireless data transmission such as the 402-405 MHz, 174-216 MHz, or 88-108 MHz bands allocated for medical implant communication services. In this system, neural activities from multiple channels are detected using two-dimensional or three-dimensional microelectrodes. After preconditioning, the multiple parallel channels are multiplexed in the frequency domain within the FDM module. As a result of FDM, preconditioned neural signals are placed in the frequency domain with 100kHz spacing, occupying a 1600kHz bandwidth starting from 10MHz. Finally, the resulting FDM band is shifted in the frequency domain by the frequency modulation (FM) block with a carrier frequency of 100 MHz. A 16-channel prototype system is designed and simulated using 0.18 µm CMOS technology, with a chip area of 0.55 × 0.58 mm^2 and a power consumption of 3.35 mW at a supply voltage of 1.8V.

E-ISSN: 3060-6357

Introduction

In recent decades, intra-cortical neural recording systems have captivated researchers in the medical and neuroscience fields, as understanding the brain's operations and its control over the body necessitates analyzing signals from neurons and deciphering their communication throughout the body. Indeed, one significant reason for the rapid advancement in neuroscience is the quest to uncover the brain's hidden secrets, which can inspire progress in a variety of scientific domains including medicine, biology, genetics, biomedical engineering, electrical engineering, robotics, and computer sciences. This is largely due to the ability of such research to open a new window into the brain, enabling researchers to explore previously unknown aspects of the nervous system and to help scientists decipher complex correlations between brain activities and the external world. The primary aim of this research was to develop practical solutions for individuals who are unable to use their body parts normally due to conditions such as spinal cord injuries, arteriosclerosis or brain disorders affecting functions like vision, hand movements and arm movements. Success in this field holds promise for advancements such as systems that can process brain signals to interface with impaired organs or artificial prostheses, thereby improving the quality of life for affected individuals [1-4]. For this reason, recent years have seen significant advancements in recording nerve signals, with the development of systems evolving from simple, single-channel, unidirectional, non-implantable wired systems to complex, bidirectional, multi-channel, implantable, and wireless systems.

Recent technological advancements have significantly contributed to this progress. Innovations in low-noise, low-power ASIC design, modulation methods, optimization techniques, and data volume reduction algorithms have all played crucial roles. However, several challenges and limitations persist in implementing these systems within medical and neuroscience contexts including issues with probe design, limitations on the number of signal recording channels, noise reduction, bandwidth constraints, high power consumption, system size, wireless transmission, and other physical considerations. Despite these hurdles, the field continues to advance, driven by the potential to create improved living conditions for individuals with disabilities. The application of new technologies and methodologies remains central to this progress, paving the way for future breakthroughs in understanding and utilizing brain signals for therapeutic purposes [5-7]. Recent advances in neuroscience research and clinical applications increasingly demand the simultaneous recording of a multitude of brain or body spike signals. However, as the number of channels increases, it limits the bandwidth allocated to implantable systems (within the frequency

ranges of 402-405 MHz or 174-216 MHz, which are designated for biomedical engineering telemetry) [8]. Consequently, efforts have focused on increasing the channel count while developing techniques for more efficient bandwidth utilization and implementing data volume reduction algorithms. Given that a high number of neural channels is a key and effective factor in intra-cortical neural recording for most applications such as neural prostheses, early efforts have been focused on increasing the number of channels [3; 6; 7; 9].

Early in the development of these systems, various innovative architectures for implantable microsystems were proposed. E. D. Adrian was the first to use instruments sensitive enough to record from single axons of sensory receptor neurons [10]. Other interesting research carried out at that time includes a wireless neural signal recording system featuring 100 electrodes for spike detection and neural signal transmission [11]. In [12], a 64-channel neural signal recording microsystem with spike feature detection capability is proposed, which transmits only the pertinent information from each channel, along with its address, to the external world. Continuing the evolution of these microsystems, researchers have turned to neural signal compression algorithms and automatic neural signal feature detection methods to expand the channel count, optimize bandwidth usage, and reduce power consumption. For example, in 2023, a 16-channel adaptive compression engine utilizing channel shifting in low-power neural signal regions was proposed, achieving approximately 78% power savings [12]. Additionally, an automatic spike detection method utilizing a spike mask was developed. This method allows multiple electrodes to share a limited number of channels, effectively increasing the total number of received channels while reducing power consumption [13; 14]. In recent years, significant efforts have been made to improve spike detection capabilities by employing compression and adaptive algorithms, feature detection methods, and neural processing techniques. These efforts, coupled with the use of advanced and up-to-date technologies, aim to increase the number of neural recording channels while optimizing power management [15-18]. Another approach in the development of these microsystems is to increase the number of channels using various multiplexing techniques to optimize bandwidth usage. For instance, the microsystems reported in [[19-23]are examples of such systems. In [21; 23; 24], techniques such as pulse width modulation (PWM) and pulse interval width modulation (PIWM) are utilized for channel combination [19]. In [20], modulation techniques and channel combinations in the time domain (TDMA) are also employed. The use of time-division multiplexing combined with advanced algorithms, in addition to cutting-edge IC fabrication technology, has created favorable conditions for enhancing wireless communication capabilities.

This approach has simultaneously led to reduced power consumption, minimized system size, and a significant increase in the number of communication channels [22; 25]. Moreover, frequency domain channel combination techniques (FDMA) [26; 27] and frequency-time division multiplexing (FDM-TDM) [28] have also been employed to increase the number of channels. The combination of optical and fiber techniques, the use of active graphene electrodes in multiplexing methods, and the implementation of digital multiplexers and neural processing algorithms have led to significant improvements in these technologies. These advancements not only increase the number of channels but also lead to a reduction in hardware volume, system size, and power consumption. Furthermore, these approaches contribute to a reduction in noise and interference in wireless communications and provide better conditions for signal reconstruction at the receiver [29-31].

In the current research, a 16-channel neural recording system based on frequency multiplexing was designed and simulated to simultaneously record signals from 16 channels of the central brain membrane. In the proposed system, while increasing the number of channels, the bandwidth allocated for wireless data transmission (the band 402-405MHz allocated to medical implant communications services or the band 174-216MHz allocated for biomedical telemetry devices) was used more effectively.

System description

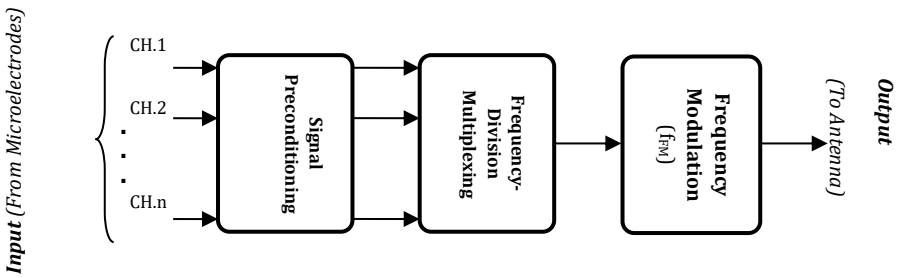


Figure 1. Block diagram of the proposed architecture [26].

The escalating demand to increase the number of channels recorded in implantable microsystems in the field of research as well as the limitations and challenges in increasing the channels of microsystems and the necessity of real-time signal transmission led the present research authors to use the FDM technique to enhance the channel count in implantable microsystems. Figure 1 shows the simplified block diagram of the proposed system. Two or three-

dimensional microelectrodes capture neural activities on multiple channels. The neural signals sensed from the probes are usually low in amplitude (about 50-500 μV). They enter the signal preconditioning module for initial processing. This module performs pre-amplification with a gain of 40~60 dB along with band-pass filtering with less than 1-Hz and around 10-KHz low and high cut-off frequencies, respectively to eliminate high-frequency noise and unwanted low-frequency signals. After preconditioning, the multiple parallel channels are then multiplexed in the frequency domain in the FDM module.

As a result, as shown in Figure 2, neural channels are transferred to frequencies $f_1, f_2, \ldots f_n$ with a bandwidth of BW_{CH}, and are placed next to each other with a certain distance, i.e., Δf: $f_2=f_1+\Delta f$, $f_3=f_2+\Delta f$, $f_4=f_3+\Delta f$,..., *and* $f_N=f_{N-1}+\Delta f$. Finally, they are combined to make an FDM signal. This signal is subsequently modulated using FM modulation (within the frequency range of 88-108 MHz) and transmitted outside the body.

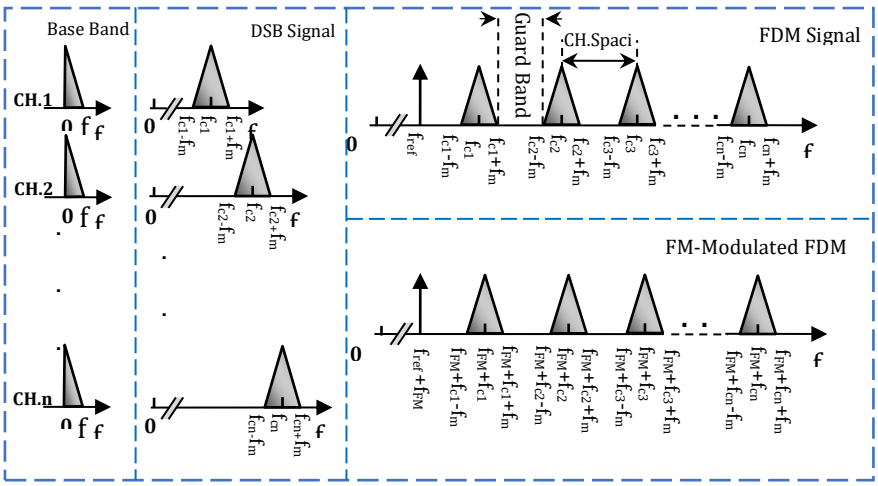


Figure 2. Neural channels are shifted to frequencies $f_1, f_2, \ldots f_n$.

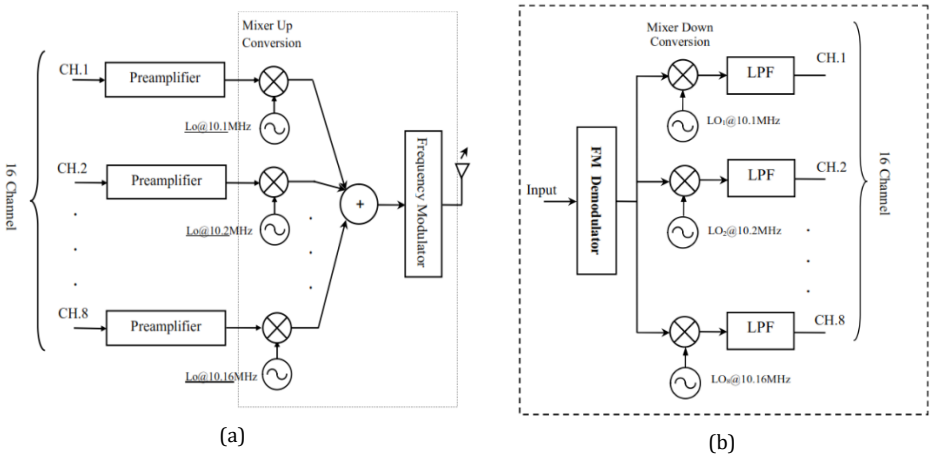


Figure 3. System block diagram (a) transmitter and (b) receiver.

Figures 3(a) and 3(b) show the simulated system in MATLAB software, depicting the transmitter and receiver sections, respectively. In the transmitter section, preamplification is performed in MATLAB software, and the neural signals from each channel are then called and filtered using a band-pass filter with a high cut-off frequency of 20 kHz and a low cut-off frequency of 4 kHz. The signals are then shifted to frequencies of 10, 10.1, ..., and 10.16 MHz using double-sideband (DSB) amplitude modulators (each channel is spaced 100 kHz from the adjacent channel to avoid interference and noise). The signals are then combined by a summing block to form the FDM signal. The FDM signal is modulated by an FM modulator at a frequency of 100-108 MHz and transmitted outside. In the receiver section, the received signal is demodulated and then shifted to lower frequencies using down-converting mixers. Subsequently, the inverse FDM process is performed, and the signals are separated using filters.

Circuit description

In this section, various components of the circuit design are presented. These components include the design of the synthesizer, current-mode analog adder, and FM modulator, which are discussed below.

Synthesizer

The critical issue is the achievable accuracy for the per-channel local oscillators generating f_1, f_2, ..., and f_N in Figure 2. Equal spacing between the channels is important, especially when demultiplexing the channels on the external side of the wireless link. To overcome this issue, a multi-output frequency synthesizer scheme is used. The simplified block diagram of the

synthesizer, designed based on the scheme presented in [32], is shown in Figure 4(a).

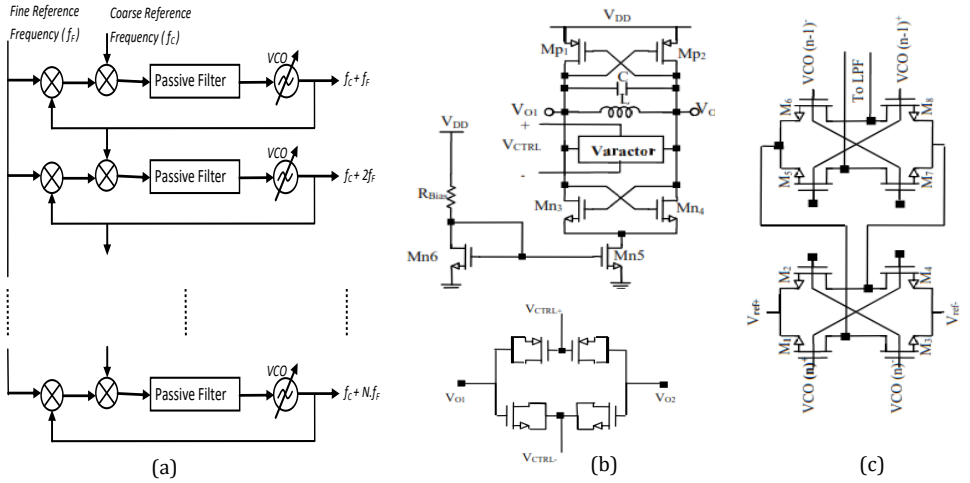


Figure 4. (a)Block diagram of the frequency synthesizer [32]; (b) VCO; (c) the passive differential mixers [33].

In this design, two fixed-frequency reference oscillators are used to define both the coarse and fine values for all local frequencies, i.e., f_C and f_F, respectively. This topology employs 16 PLLs, with central frequencies controlled by two external reference frequencies. To enhance central frequency accuracy and maintain frequency spacing between adjacent signals, the external signal frequencies are set to F_f=10MHz and F_c=100kHz. Therefore, the PLLs output frequencies are 10.1, 10.2, ..., and 10.16 MHz. Figures 4(b) and 4(c) depict the circuits constituting this synthesizer, designed differentially to mitigate environmental and power supply noise, as well as second-order harmonics. In addition, to realize the mixers shown in Figure 4(c), passive differential mixers are utilized [33].

Analog adder

Figure 5 shows the block diagram of an analog adder. In this block diagram, the input voltages are first converted to current by the voltage-to-current converter. The resulting currents are then summed and finally converted back to voltage by the current-to-voltage converter block.

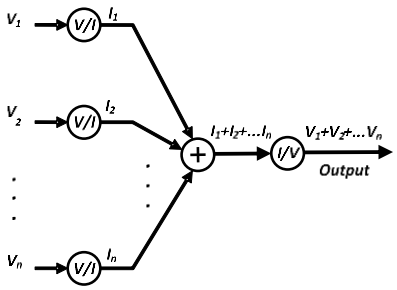


Figure 5. Block diagram of analog adder.

Figure 6 shows a schematic of the analog adder used in the FDM module. In this circuit, the 16-channel differential input voltages are first converted to currents by differential circuits. As an example, for two inputs, it can be written as follows:

$$i_{dM1} = k(v_{GSM1} - v_{th})^2 \quad [(v_{GSM!} = v_{c1} + \frac{v_{d1}}{2} - v_x)\&(v_{in1} = v_{iM1} - v_{iM2})] \tag{1.a}$$

$$i_{dM2} = k(v_{GSM2} - v_{th})^2 \quad [(v_{GSM2} = v_{c1} - \frac{v_{d1}}{2} - v_x)\&(v_{in1} = v_{iM1} - v_{iM2})] \tag{1.b}$$

$$i_{dM3} = k(v_{GSM3} - v_{th})^2 \quad [(v_{GSM3} = v_{c2} + \frac{v_{d2}}{2} - v_y)\&(v_{in2} = v_{iM3} - v_{iM2})] \tag{1.c}$$

$$i_{dM4} = k(v_{GSM4} - v_{th})^2 \quad [(v_{GSM4} = v_{c2} - \frac{v_{d2}}{2} - v_y)\&(v_{in2} = v_{iM3} - v_{iM2})] \tag{1.d}$$

Then, the currents at nodes A and B are combined, which can be written as:

$$i_{dMo1} = i_{dM1} + i_{dM3} \ , \ i_{dMo2} = i_{dM2} + i_{dM4} \tag{2}$$

The added currents in the final stage are then converted into voltage, which is:

$$v_{out} = r_{out} * i_{dMo1} \quad [r_{out} = r_{oP} \parallel r_{oN}] \tag{3}$$

Therefore, according to reference [34], if the dimensions of the output transistors are greater than those of the input transistors and the bias currents for all transistors are the same, the linear performance of this topology can be assured. Therefore, it can be written as:

$$v_{out} = v_{d1} + v_{d2} \tag{4}$$

Current-mode analog adder choice of a differential and current-based structure aims to eliminate noise, interference, and second-order harmonics.

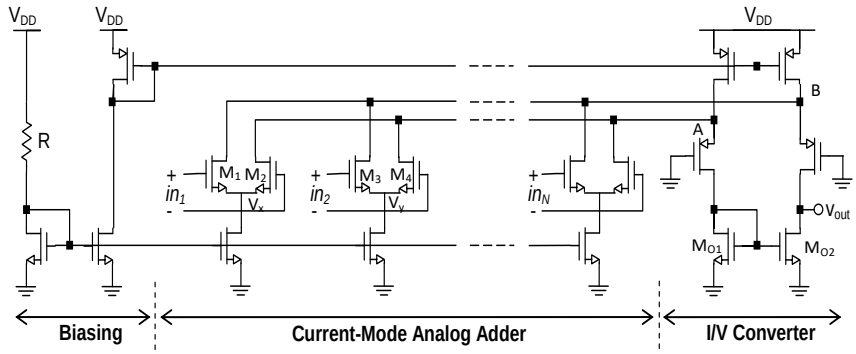


Figure 6. Circuit schematic of the current-mode analog adder [26].

FM Modulator

Figure 7 presents the schematic of the frequency modulator, employed as an FM transmitter in the system. This modulator includes a Colpitts oscillator with an LC tank circuit, a capacitor, and a MOS varactor, operating within the frequency range of 88-108 MHz. Off-chip components (L, C_1, C_2) are chosen to reduce system power consumption and ensure faster oscillation frequency stabilization (due to high Q factor). Additionally, a programmable resistor (R_B) within the range of 2-7 kHz controls the bias current of transistor M_1.

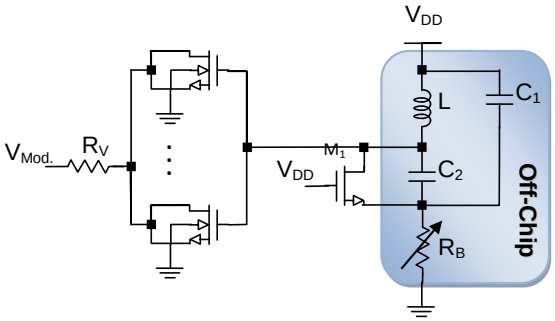


Figure 7. Schematic diagram of FM modulator [26].

Results and discussion

To evaluate the proposed idea, a 16-channel system was designed and simulated at both the system and transistor levels. Neural signals recorded from the auditory cortex of a guinea pig were used as inputs to all the channels. Figure 8 illustrates the four input neural channels of the transmitter and the four output neural channels of the receiver in the system simulation conducted using MATLAB software.

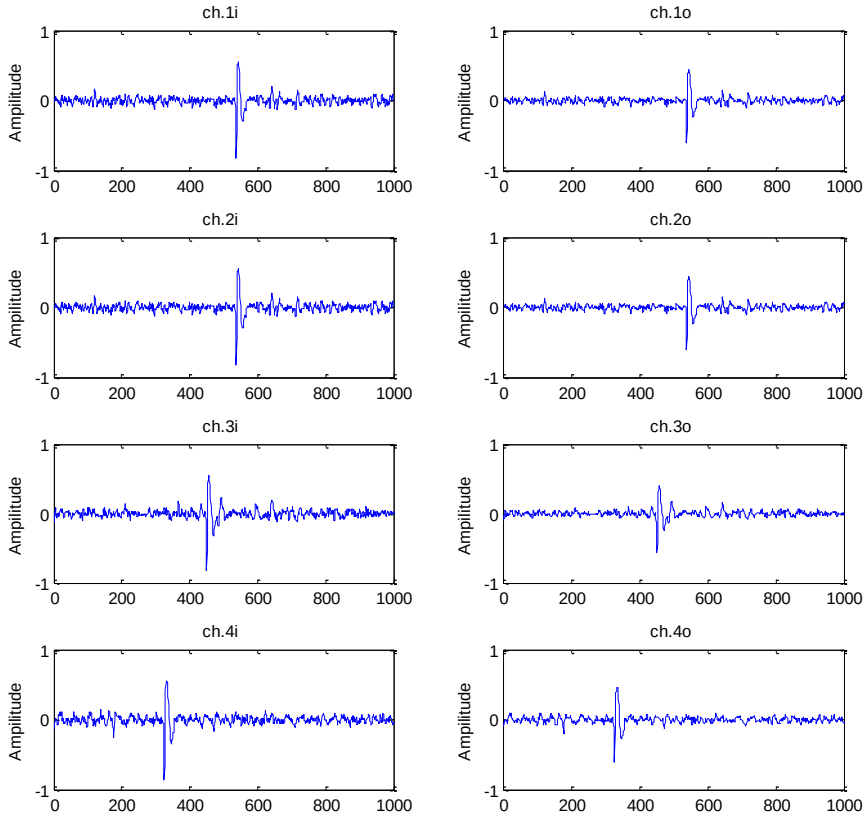


Figure 8. Input signals at transmitter and output signals retrieved on the external side of the wireless link after frequency demodulation, frequency-division demultiplexing, and filtering.

Additionally, Figure 9 shows the input and output signals of a single channel of the introduced microsystem simultaneously.

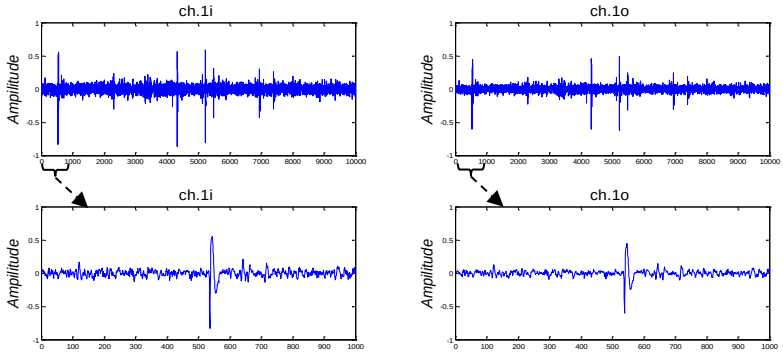


Figure 9. Input neural signal on the transmitter and the signal retrieved on the receiver at system levels.

To evaluate the circuit designed at the transistor level, device parameters from a standard 0.18 µm CMOS process were used. Figure 10 shows the input and recovered output signals on the external side of the system simultaneously as obtained from the transistor-level simulation.

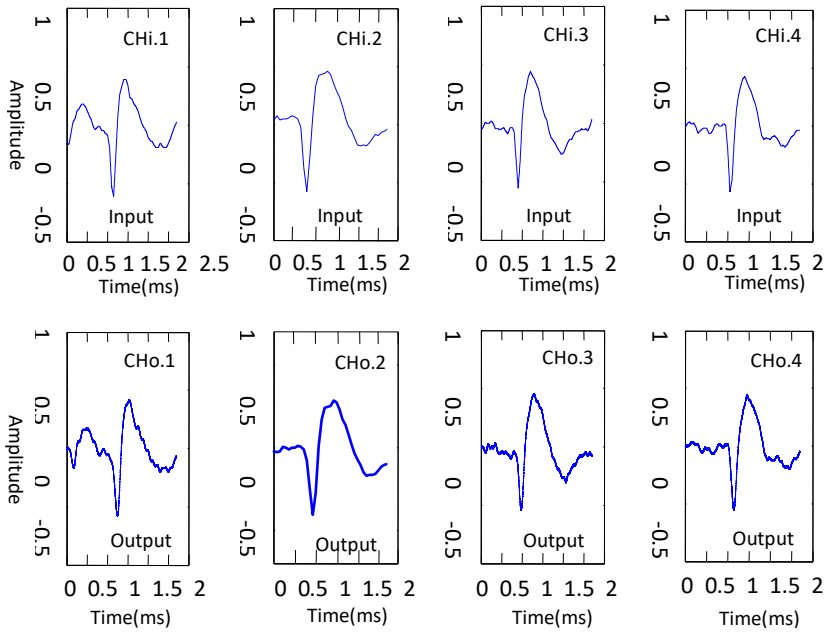


Figure 10. Input neural signal on the transmitter and the signal retrieved on receiver transistor levels.

Figure 11 illustrates the output signal of the analog adder circuit used in the FDM module in the frequency domain as a result of the circuit simulation. Notably, the largest signal amplitude resulting from the non-linear behavior of the analog adder circuit was -60 dB, negligible compared to the original signals in the summation process. In addition, a gain of 15 dB was incorporated in the analog adder circuit design to minimize losses in the mixer. The power consumption of the circuit was measured to be 1.092 mW.

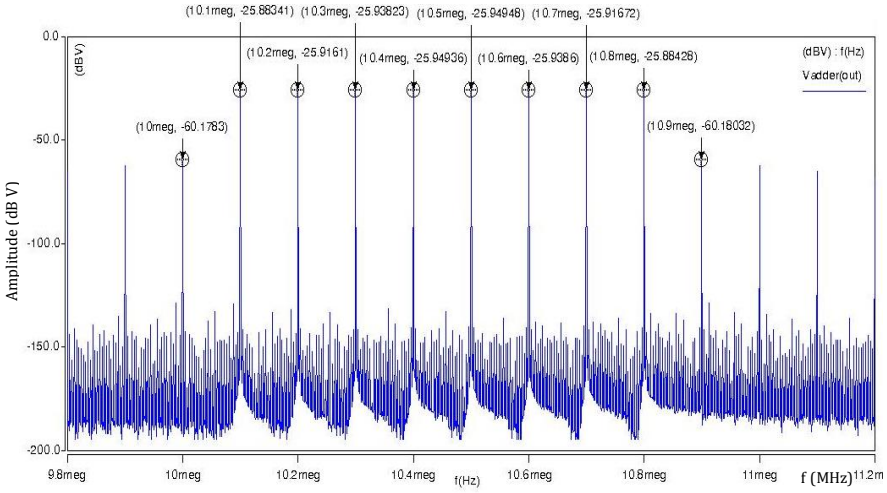


Figure 11. Simulated output spectrum of the analog adder circuit for 8 Channels.

There are interrelated parameters impacting the performance of the demodulator in the receiver unit. To achieve optimal performance, these parameters must be evaluated on the transmitter side, considering the existing constraints. Among these parameters is the dynamic range of the FM modulator, which is depicted in Figure 12.

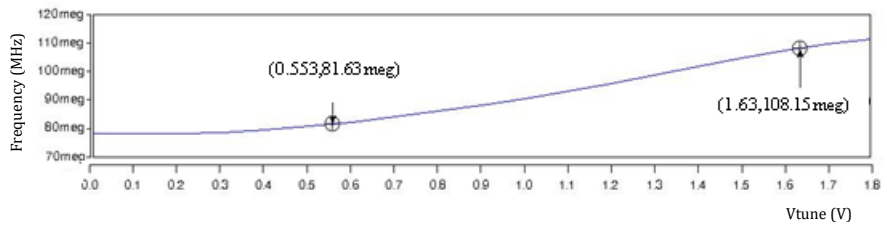


Figure 12. Frequency variation curve as a function of voltage in the FM modulator.

Based on the simulation results, the FM modulator's dynamic range was 26.5 MHz, and its gain was measured as 25.7 MHz/V. Another significant parameter in the modulator was harmonic distortion from the first to the third order and total harmonic distortion (THD), which were analyzed according to Equation 5 and the modulator's output spectrum shown in Figure 13.

$$THD = \frac{\sum_2^n |\, v_{on}|}{v_{o1}} \tag{5.a}$$

$$HD_n = \frac{v_{on}}{v_{o1}} \tag{5.b}$$

Where V_{on} represents the harmonic amplitude and V_{o1} represents fundamental harmonic amplitude.

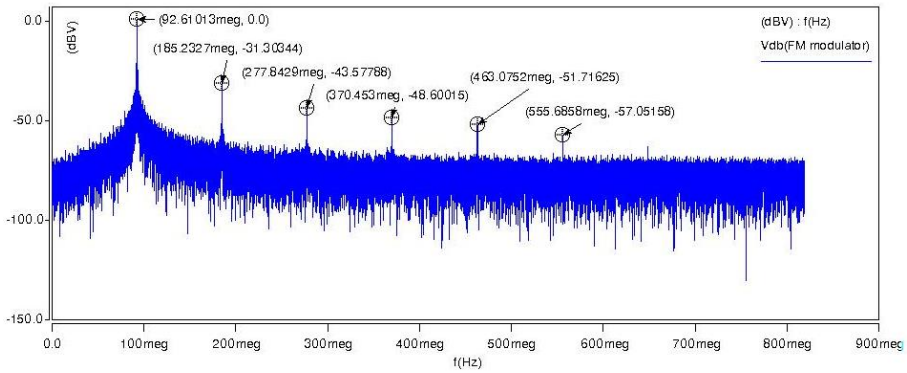


Figure 13. Simulated Output Spectrum of the FM modulator.

Based on Figure 13, the first-order harmonic distortion coefficient (HD1) was measured to be 2.81%, the second-order harmonic distortion coefficient (HD2) was 0.5%, and the third-order harmonic distortion coefficient (HD3) was 0.4%. Additionally, the total harmonic distortion (THD) of the output sinusoidal signal was measured to be 2.87%. The modulator's power consumption in the simulation with a supply voltage of 1.8 V, was measured at 1.068 mW.

The 16-channel prototype system was designed and simulated with 0.18 µm CMOS technology and a chip area of 0.55*0.58 mm^2, consuming 3.354 mW at 1.8V supply voltage.

Considering the importance of power efficiency in implantable microsystems, Table 1 illustrates a detailed comparison of the measured power consumption across the various modules of the designed system. Moreover, Figure 14 depicts the power consumption percentage for each subsystem. As indicated in Figure 14, the frequency synthesizer accounts for the highest power consumption, making it the most power-demanding component in the system.

Table 1. Power consumption across the various modules.

Components	Power consumption
Analog adder	1.092 mW
Mixer	64 uW
Fm modulator	1.068 mW
Synthesizer	1.13 mW
System	3.354 mW

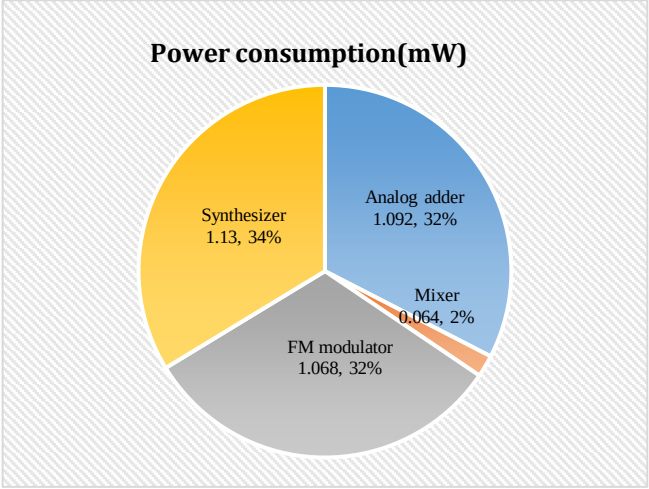


Figure 14. Power consumption percentage of different units.

Experimental results

Although the system was prepared for microfabrication, a 4-channel macro-scale prototype of the system was realized using off-the-shelf components to examine its functionality (Figure 15). In this system, the AD835 IC was utilized as an analog multiplier operating in double-sideband (DSB) mode to upconvert the baseband signal frequency.

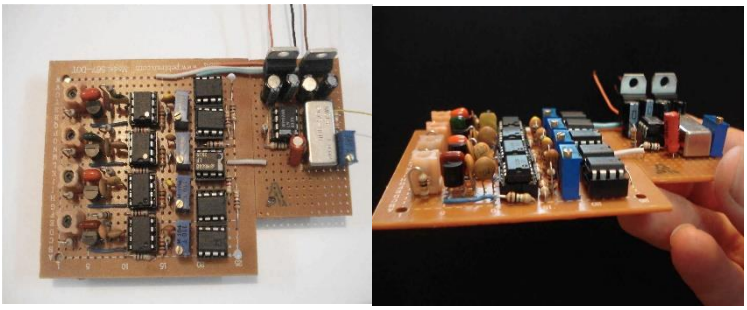


Figure 15. Macro-version of the system realized using off-the-shelf components.

The local oscillator (LO) signal, required for the Frequency Division Multiplexing (FDM) block, was generated by a Colpitts oscillator and then filtered using second-order active filters to ensure signal purity. The signals from each channel, after modulation and upconversion to a higher frequency, were combined using an analog adder implemented with an operational amplifier (op-amp). The resulting combined signal was transmitted wirelessly via an FM modulator, which was implemented using a high-bandwidth voltage-controlled oscillator (VCO) (POS100). The transmitted signal was then received by a radio receiver and displayed on an

oscilloscope for analysis. Note that the frequency separation between adjacent channels in each oscillator was set to approximately 60 kHz. Thus, the channels were positioned at the base band frequencies of 60 kHz, 130 kHz, and 200 kHz.

The system was evaluated and tested using both sinusoidal and spike signals. In the initial phase of this test, sinusoidal signals with a frequency of approximately 7 kHz were input into the system, and the signals were received and demodulated at a distance of two meters. Figure 16 shows the frequency-domain representation of the transmitted and received signals for a single channel.

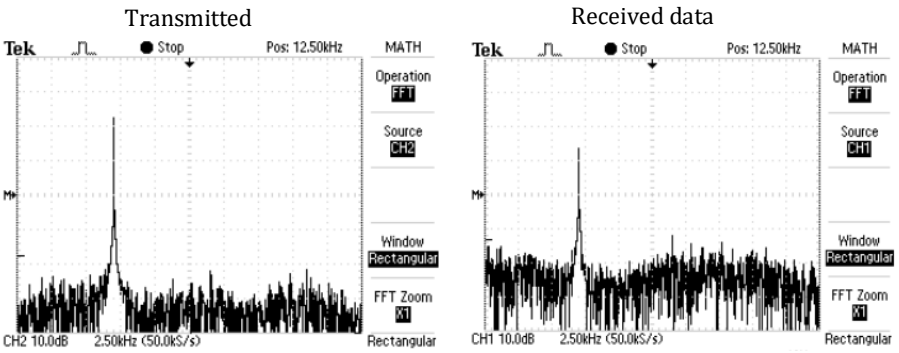
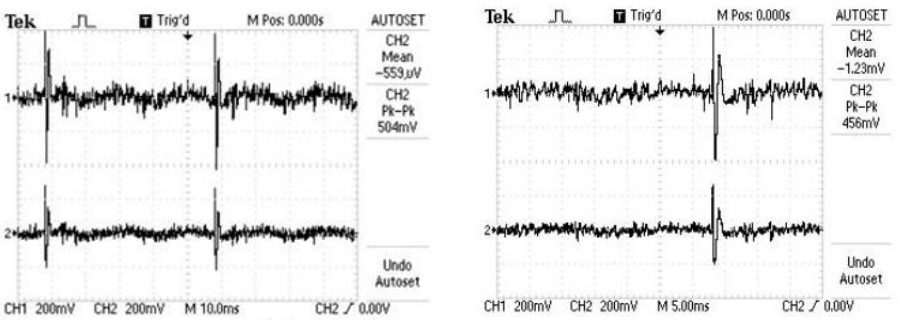


Figure 16. Oscilloscope screenshots showing the input and output spectra of a sinusoidal signal.

In the second phase, pre-recorded neural signals were input into the system through an interface card connected to a computer. Figure 17 illustrates oscilloscope screenshots showing both the neural input signal to the system and the recovered signal on the receiver side of the wireless link.



(a) (b)

Figure 17. Oscilloscope screenshots displaying both the input neural signal on the system side and the corresponding signal recovered on the external side of the wireless link: (a) wide view; (b) detailed view of an action potential.

Conclusion

This paper presents a 16-channel architecture for multi-channel implantable microsystems, where frequency division multiplexing (FDM) was used to combine the system's channels. The main advantage of this approach is that it increases the number of channels in implantable systems and allows for the uninterrupted transmission of the entire recorded nerve signal activity. This is in contrast to most neural signal recording systems, which focus on transmitting only certain characteristics of neuronal signals. This architecture opens a new avenue for increasing the number of channels in multi-channel neural recording microsystems, which can serve as a foundation for numerous activities and research in the field of implants. However, despite the advantages, there are several challenges to achieving a fully functional implant system. These include issues such as the high number of off-chip components, the need for precise external signal requirements to stabilize oscillator frequencies, the complexity of PLL design, increasing power consumption with more channels, noise issues, and the non-linear characteristics of selection blocks. These challenges present opportunities for new activities and research in the continuation of this work.

Disclosure statement and funding

The authors declare no potential conflicts of interest. The present study received no financial support from any organization or institution.

Acknowledgment

We would like to give special thanks to all the participants in this study.

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